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Applicants: Kianian et al.

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**U.S. PATENT DOCUMENTS**

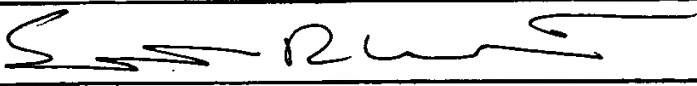
Examiner Initial	Patent No. Publication No.	Date	Name	Class	Sub-class	Filing date if appropriate
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**FOREIGN PATENT DOCUMENTS**

Document number	Date	Country	Class	Sub-class	Translation YES NO

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

SW	SZE, Simon, "Physics of Semiconductor Devices", 2nd Edition, Wiley-Interscience, Basic Device Characteristics, pages 438-439.
SW	BROWN, William D., et al.; "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide To Understanding And Using NVSM Devices", IEEE Press, pages 33-34.
SW	HAYASHI, et al., "A Self-aligned Split-Gate Flash EEPROM Cell With 3-D Pillar Structure," 1999 Symposium on VLSI Technology Digest of Technical Papers, pp. 87-88, Center for Integrated Systems, Stanford University, Stanford, CA 94305, USA.

Examiner: 	Date Considered: 12/8/2004
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